# TMC2069P7C

## Demonstration Board for the TMC3003 DAC

### Features

- Parallel TTL Compatible Inputs
- Component and VGA Outputs
- Raytheon demo board compatibility

### Applications

- Evaluation of TMC3003 DAC
- Output for TMC2068P7C Decoder demo board
- Output for Genesis 10-bit Line doubler board
- System Breadboarding

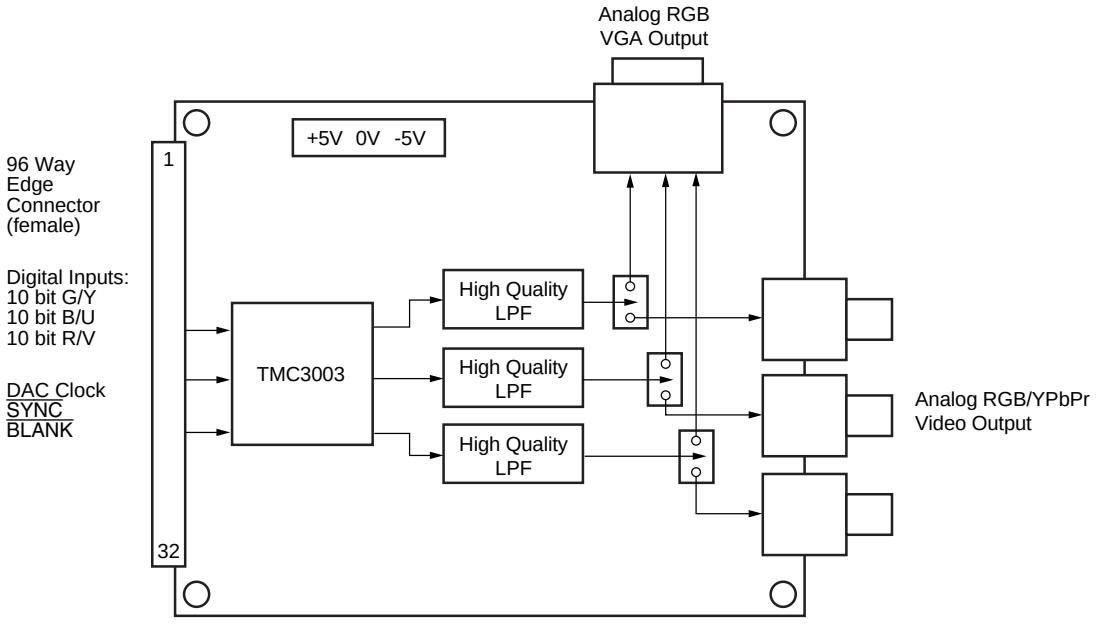
### Description

The TMC2069P7C DAC demonstration board provides a flexible base for evaluating the performance of the TMC3003 triple 10 bit DAC.

The board can output analog component video or VGA. There are high quality Sanders Media Adventure Hybrid filters (SMA 601-003) on the output.

**Preliminary Information**

### Block Diagram




**Analog Outputs for the TMC22153 Digital Decoder**



**PRELIMINARY INFORMATION** describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact Raytheon Electronics for current information.

Preliminary Information

## Functional Description

The TMC2069P7C is designed to demonstrate the performance of the TMC3003 Digital to Analog converter. It also offers an example of design practices that result in high-quality video performance.

The TMC3003 is a high-speed triple 10-bit D/A converter especially suited for video and graphics applications. It offers 10-bit resolution, TTL-compatible inputs, low power consumption, and requires only a single +5 Volt power supply. It has single ended current output, $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ control inputs, and a separate current source for adding sync pulses to the Green D/A converter output. It is ideal for generating analog RGB from digital RGB and driving computer display and video monitors. Three speed grades are available: 30, 50, and 80 Msps.

The DAC module can be plugged into the TMC2068P7C decoder demonstration board to provide analog RGB or YPbPr outputs for viewing the decoder performance. The board can also be plugged into the 10-bit DICE line doubler demonstration board from Genesis. The input for the Genesis 10 bit line doubler board is being provided by the TMC2067P7C 10 bit ADC demonstration board connected to the TMC2068P7C decoder demonstration board.

A set of switches routes the triple DAC outputs to either the VGA connector or the component video connectors. The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ signals to the triple DAC are required for the VGA mode are disabled when the component video output is required. The component video connectors provide sync on green.

## Setup Procedure

1. To set up the output levels on the triple dac, place a digital NTSC unmodulated ramp that has peak white at the digital level 824 and blanking at 240.

2. The output analog levels should be 286 mV sync tip to blank level and 1.0V sync tip to peak white. If the output levels are incorrect, adjust the GREEN output using the potentiometer RV1.

3. Apply either the unmodulated digital ramp used in step 1 to the red and blue inputs to adjust the Pb/BLUE and Pr/RED outputs or apply SMPTE color bars and measure the Pb and Pr outputs.

4. Adjust RV2, to adjust the RED, and RV3, to adjust the BLUE output.

   a. If using the unmodulated ramp, match the output voltage levels to the values on the green channel.

   b. If using the SMPTE color bars, the level of Pb and Pr peak to peak should be 525 mV.

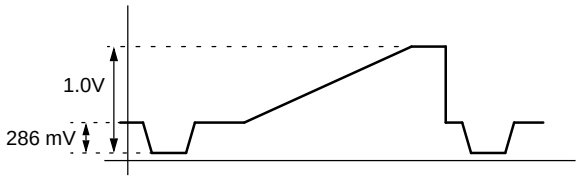



**Figure 2. Unmodulated Ramp Waveform**

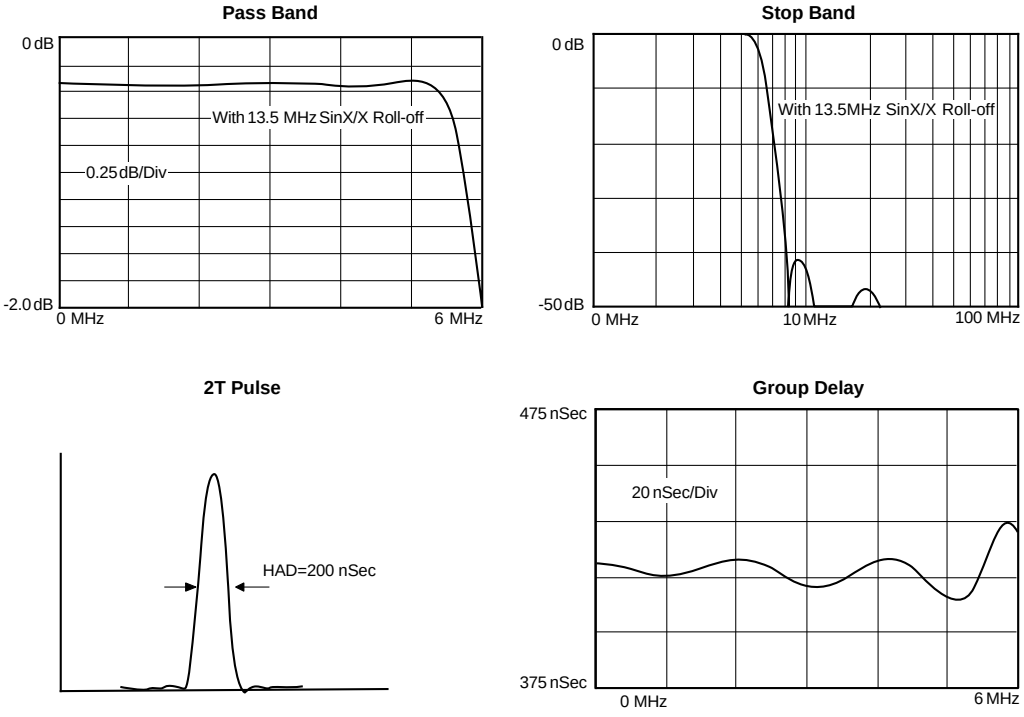



**Figure 1. Output Low Pass Filters**

## Power Supply Requirements

The TMC2069P7C board requires 1.5 Amps from the +5 Volt power supply and 0.5 Amps from the -5 Volt power supply. The -5 Volt power supply powers the SMA filters. The +5 Volt power supply not only drives TTL logic devices but it also provides the power and voltage references to the TMC3003. Therefore, it is recommended that a bench power supply be used with the cable lengths kept to a minimum.

## Output Low-Pass Filters

The SMA 601-003 filters are high end broadcast quality filters. They are Virtual 601 post filters with a bandwidth of 5.75MHz. 5-pole, sharp cutoff, Elliptic response, with 3 sections of group delay equalization. These filters were designed for SinX/X compensated CCIR 601 luminance applications and make an excellent post-filter following a D/A converter.

The response at 5.0MHz typically varies<±0.25dB with supplies of ±5V to ±8V. When operating in the 0dB gain mode, pin 6 must be well isolated from ground planes. When operating in the +6dB gain mode, pin 6 must have a low resistance path to ground.

Preliminary Information

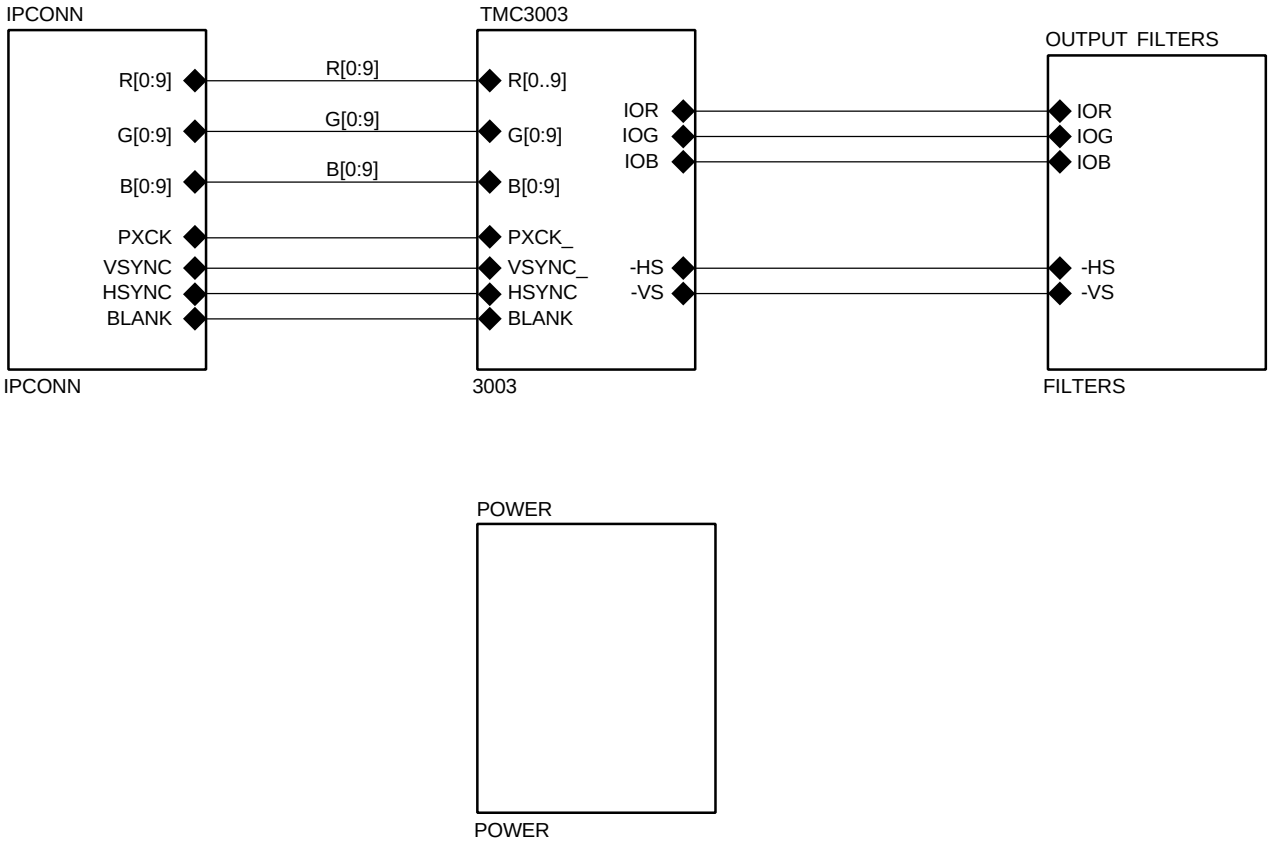



**Figure 3. TMC2069P7C (10 Bit Triple DAC)**

## Schematics (continued)

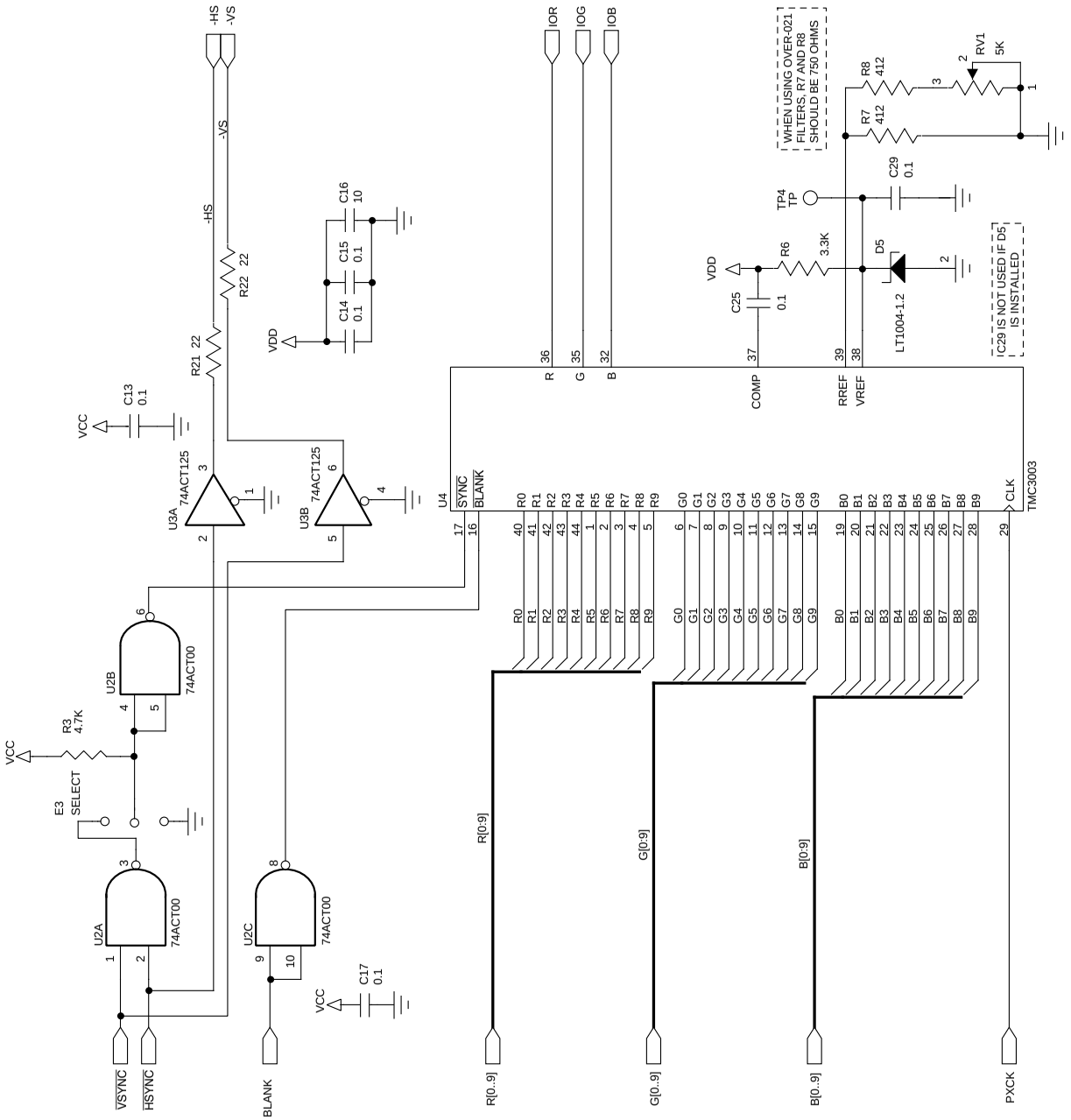



**Figure 4. TMC3003, Passive Filters**

**Preliminary Information**

## Schematics (continued)

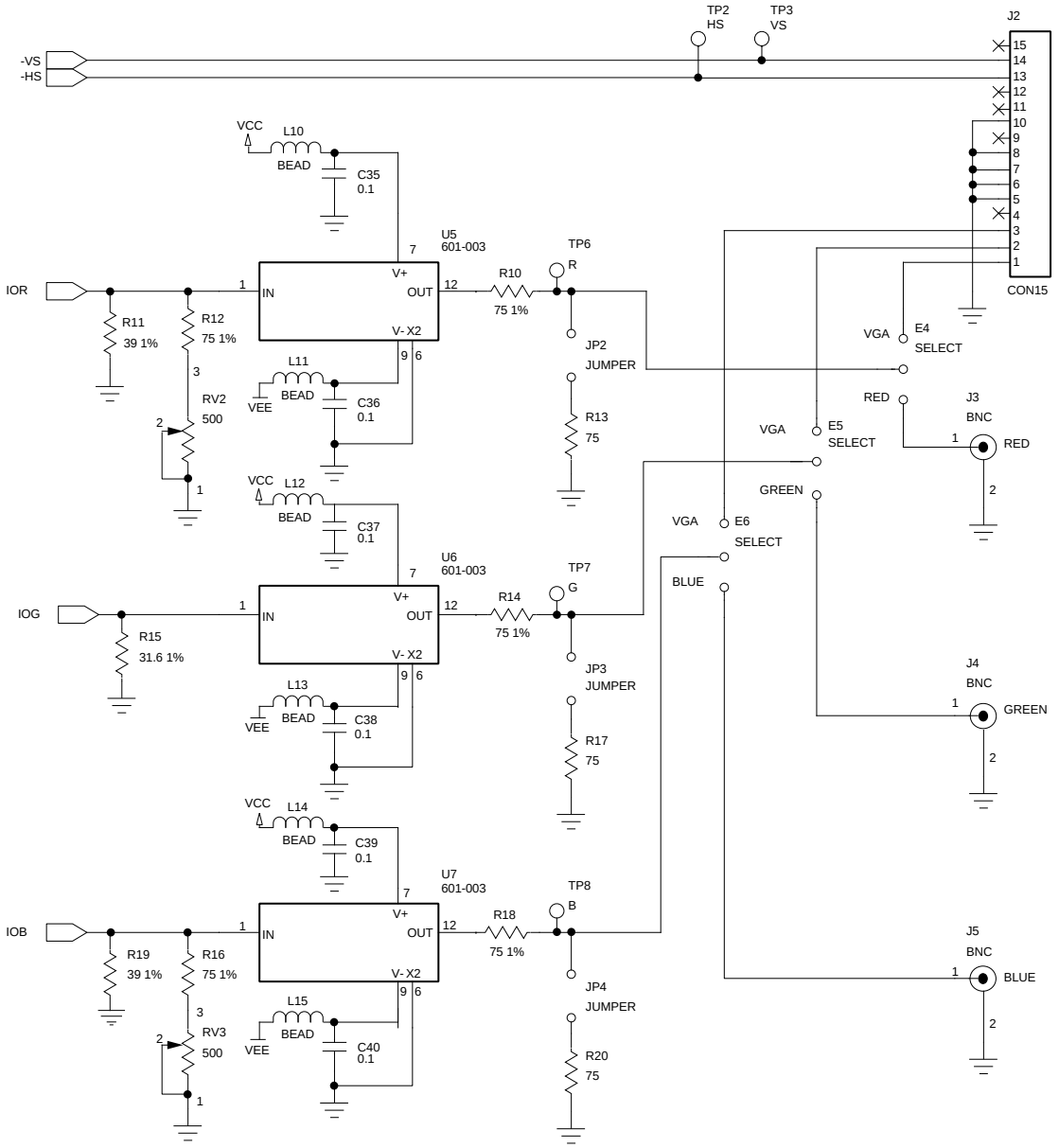



**Figure 5. TMC2069P7C**

## Schematics (continued)

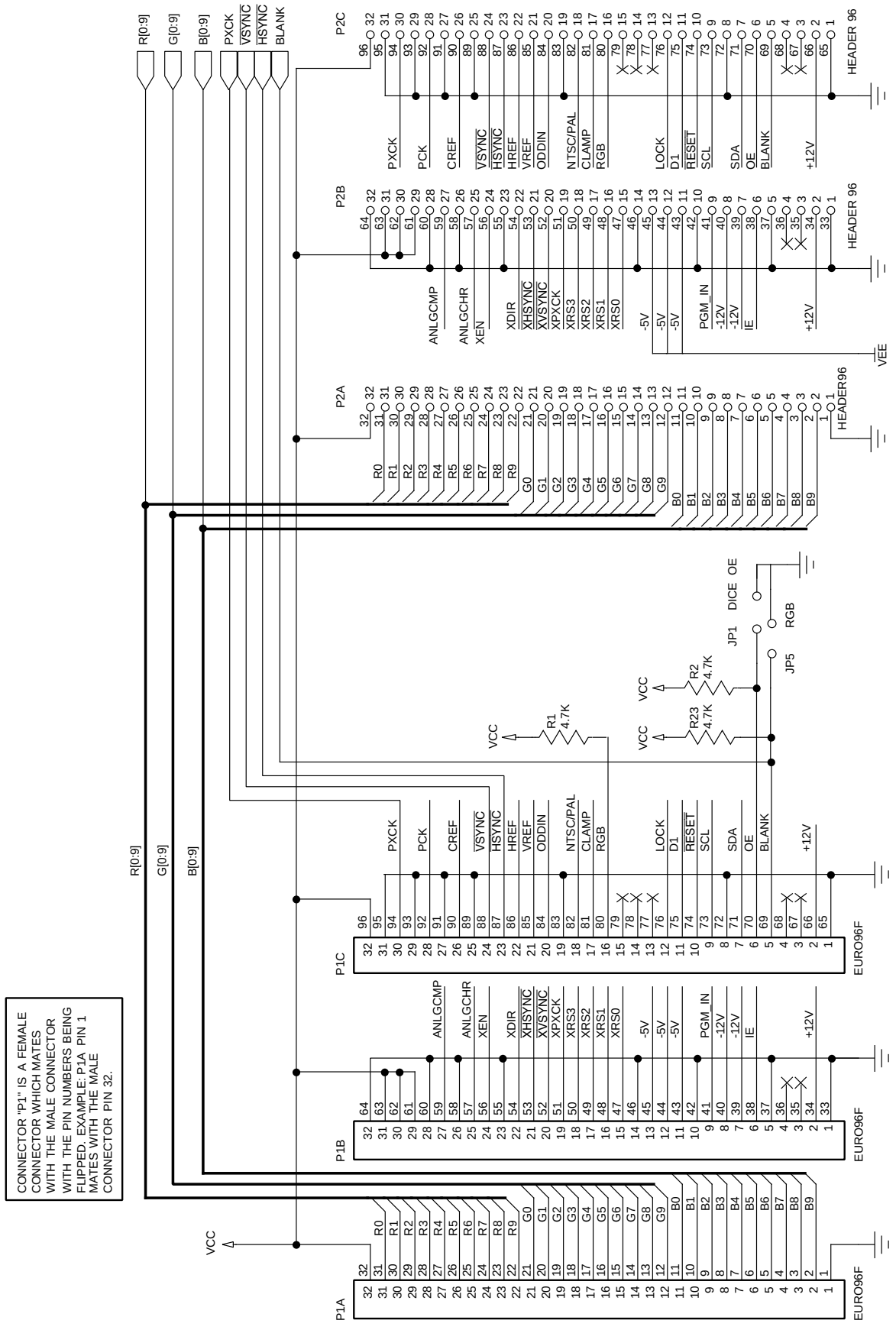



**Figure 6. IPCONN**

**Preliminary Information**

## Schematics (continued)

Preliminary Information

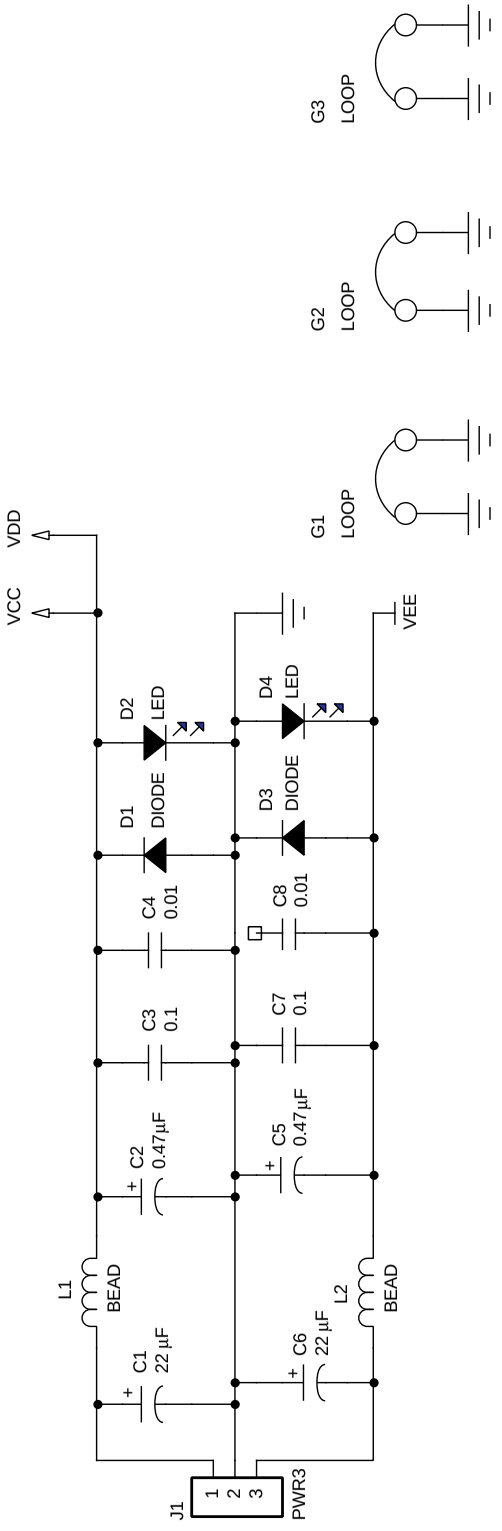



**Figure 7. Power**

**Table 1. TMC2069P7C Parts List**

| Item | Qty. | Part Name | Reference Designator | Description |
|---|---|---|---|---|
| 1 | 2 | MiniReel: 645-823 | C1,C6 | 22uf 25v Tantalum |
| 2 | 2 | MiniReel: 641-647 | C2,C5 | 0.47 uf 25v Tantalum |
| 3 | 1 | MiniReel: 644-810 | C16 | 10 uf 25v Tantalum |
| 4 | 14 | MiniReel: 605-611 | C3,C7,C13,C14,C15,C17,C25,C29, C35,C36,C37,C38,C39,C40 | 0.1uF |
| 5 | 2 | MiniReel: 605-510 | C4,C8 | 0.01 uf |
| 6 | 2 | MiniReel: 76-4004 | D1,D3 | FM4004, Diode |
| 7 | 1 | HP: hlmp-1600 | D2 | LED, Red 5v |
| 8 | 1 | HP: hlmp-1620 | D4 | LED, Yellow 5v |
| 9 | 1 | Linear Technology LT1004CH-1.235 | D5 | LT1004, 1.2 |
| 10 | 4 | SECMA: 090320102 | E3,E4,E5,E6 | Subminiature switch, 2 pos. sip |
| 11 | 3 | | G1,G2,G3 | Wire Loop, gnd |
| 12 | 5 | AMP: 103747-2 | JP1,JP2,JP3,JP4,JP5 | Jumper, header |
| 13 | 1 | BEAU: 870503 BEAU: 871803 | J1 | Terminal block plug, and socket |
| 14 | 1 | AMP: 748390-5 | J2 | Con15, VGA |
| 15 | 3 | Amphenol: 31-5431 | J3,J4,J5 | BNC, Connector |
| 16 | 8 | Fair-Rite: 2743019447 | L1,L2,L10,L11,L12,L13,L14,L15 | Ferrite Bead |
| 17 | 1 | AMP: 650461-4 | P1 | EURO96F, Connector |
| 18 | 1 | AMP: 3-103817-0 | P2 | Header-96, 3x32 |
| 19 | 1 | Bourns: 3262W502 | RV1 | 5k ohm, pot. |
| 20 | 2 | Bourns: 3262W501 | RV2,RV3 | 500 ohm, pot. |
| 21 | 4 | MiniReel: 615-848 | R1,R2,R3,R23 | 4.7k ohm |
| 22 | 1 | MiniReel: 615-844 | R6 | 3.3k ohm |
| 23 | 1 | MiniReel: 615-347 | R7 | 475 ohm |
| 24 | 1 | MiniReel: 615-375 | R8 | 750 ohm |
| 25 | 5 | MiniReel: 615-275 | R10,R12,R14,R16,R18 | 75 ohm 1% |
| 26 | 2 | MiniReel: 615-809 | R11,R19 | 39 ohm 1% |
| 27 | 3 | MiniReel: 655-275 | R13,R17,R20 | 75 ohm |
| 28 | 1 | MiniReel: 615-231 | R15 | 31.6 ohm 1% |
| 29 | 2 | MiniReel: 615-804 | R21,R22 | 22 ohm |
| 30 | 6 | Mouser: ME151-203-100 | TP2,TP3,TP4,TP6TP7,TP8 | Test Points |
| 31 | 1 | Motorola: 74ACT00 | U2 | surface mount IC |
| 32 | 1 | Motorola: 74ACT125 | U3 | surface mount IC |
| 33 | 1 | Raytheon: TMC3003 | U4 | surface mount IC |
| 34 | 3 | Sanders: 601-003 | U5,U6,U7 | Active filters |
| 35 | 2 | CCI: B500-2-0.5-FO | Shield | Board stiffener used as a shield Special order part |

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Preliminary Information

### INPUT 96 Way Connector (Female)

| Row A | | Row B | | Row C | |
|---|---|---|---|---|---|
| 32 | +5V | 32 | GND | 32 | +5v |
| 31 | D1 or R/V [bit 0] | 31 | +5V | 31 | GND |
| 30 | D1 or R/V [bit 1] | 30 | +5V | 30 | PXCK |
| 29 | D1 or R/V [bit 2] | 29 | +5V | 29 | GND |
| 28 | D1 or R/V [bit 3] | 28 | GND | 28 | PCK |
| 27 | D1 or R/V [bit 4] | 27 | Analog Composite/luma | 27 | GND |
| 26 | D1 or R/V [bit 5] | 26 | GND | 26 | CREF |
| 25 | D1 or R/V [bit 6] | 25 | Analog chroma | 25 | GND |
| 24 | D1 or R/V [bit 7] | 24 | XEN | 24 | $\overline{\text{VSYNC}}$ |
| 23 | D1 or R/V [bit 8] | 23 | GND | 23 | $\overline{\text{HSYNC}}$ |
| 22 | D1 or R/V [bit 9] | 22 | XDIR | 22 | HREF |
| 21 | Comp, G/Y, or Luma [bit 0] | 21 | $\overline{\text{XHSYNC}}$ | 21 | VREF |
| 20 | Comp, G/Y, or Luma [bit 1] | 20 | $\overline{\text{XVSYNC}}$ | 20 | ODD IN |
| 19 | Comp, G/Y, or Luma [bit 2] | 19 | XPXCK | 19 | GND |
| 18 | Comp, G/Y, or Luma [bit 3] | 18 | XRS [bit 3] | 18 | NTSC/PAL |
| 17 | Comp, G/Y, or Luma [bit 4] | 17 | XRS [bit 2] | 17 | CLAMP pulse |
| 16 | Comp, G/Y, or Luma [bit 5] | 16 | XRS [bit 1] | 16 | RGB |
| 15 | Comp, G/Y, or Luma [bit 6] | 15 | XRS [bit 0] | 15 | |
| 14 | Comp, G/Y, or Luma [bit 7] | 14 | GND | 14 | |
| 13 | Comp, G/Y, or Luma [bit 8] | 13 | -5V | 13 | |
| 12 | Comp, G/Y, or Luma [bit 9] | 12 | -5V | 12 | LOCK |
| 11 | Chroma or B/U [bit 0] | 11 | -5V | 11 | D1 |
| 10 | Chroma or B/U [bit 1] | 10 | GND | 10 | $\overline{\text{RESET}}$ |
| 9 | Chroma or B/U [bit 2] | 9 | PGM_IN | 9 | SCL |
| 8 | Chroma or B/U [bit 3] | 8 | -12V | 8 | GND |
| 7 | Chroma or B/U [bit 4] | 7 | -12V | 7 | SDA |
| 6 | Chroma or B/U [bit 5] | 6 | IE (input enable) | 6 | OE (output enable) |
| 5 | Chroma or B/U [bit 6] | 5 | GND | 5 | $\overline{\text{BLANK}}$ (DAC) |
| 4 | Chroma or B/U [bit 7] | 4 | | 4 | |
| 3 | Chroma or B/U [bit 8] | 3 | | 3 | |
| 2 | Chroma or B/U [bit 9] | 2 | +12V | 2 | +12V |
| 1 | GND | 1 | GND | 1 | GND |

## Input Edge Connector Design Notes

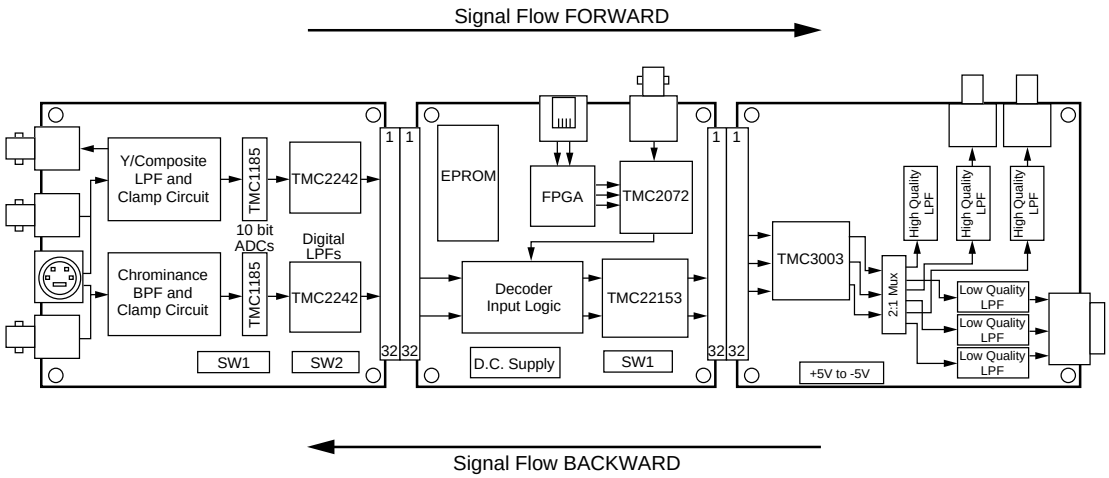


**Figure 8.**

### Important:

**Boards with different revision letters may not be compatible. Damage may occur if they are connected together!**

- XPXCK is a two times pixel clock fed BACKWARD.
- XHSYNC and XVSYNC are timing reference signals fed BACKWARD.
- The MASTER/SLAVE signal states if a board is a MASTER or a SLAVE board. This signal is fed FORWARD. A MASTER board produces the PXCK, HSYNC, and VSYNC signals, and a SLAVE board expects to receive XPXCK, XHSYNC, XVSYNC, etc .
- XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
- PGM_IN is a negative going pulse, logically ANDed with the onboard program start pulse, for initiating the programming sequence for components on that board. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. Minimum width of PGM_IN is 1uS.
- The RESET pin on the input edge connector should be connected directly to the RESET pin on the output connector. A link should be used to connect any pulse to the RESET line.
- The MASTER/SLAVE, XDIR, PGM_IN and RESET pins on the input edge connector should be connected to +5V through a 10k pull up resistor.
- The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

## Related Products

- TMC2068P7C Decoder demonstration board
- TMC2067P7C ADC demonstration board
- Raydemo software
- TMC2070P7C R-bus interface board

Preliminary Information

## Ordering Information

| Product Number | Temperature Range | Speed Grade | Screening | Package | Package Marking |
|---|---|---|---|---|---|
| TMC2069P7C | 25°C | 80 MHz | Commercial | 4” by 5” Printed Circuit Board | TMC2069P7C |
| TMC2069P7CG[1] | 25°C | 80 MHz | Commercial | 4” by 5” Printed Circuit Board | TMC2069P7CG |

**Notes:**

1. Setup for use with Genesis 10-bit line doubler and comes with SMA OVER-21 filters instead of SMA 601-003 filters.

A schematic database is available in OrCAD™ format. Contact the factory.

The TMC2069P7C Demonstration Board, design documentation, and software are provided as a design example for the customers of Raytheon. Raytheon makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

## FCC Compliance

This device has not been approved by the Federal Communications Commission (FCC). This board is intended for the evaluation of Raytheon products only. This device is not and may not be offered for sale or lease or sold or leased until the approval of the FCC has been obtained.

Preliminary Information

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